<Part F>

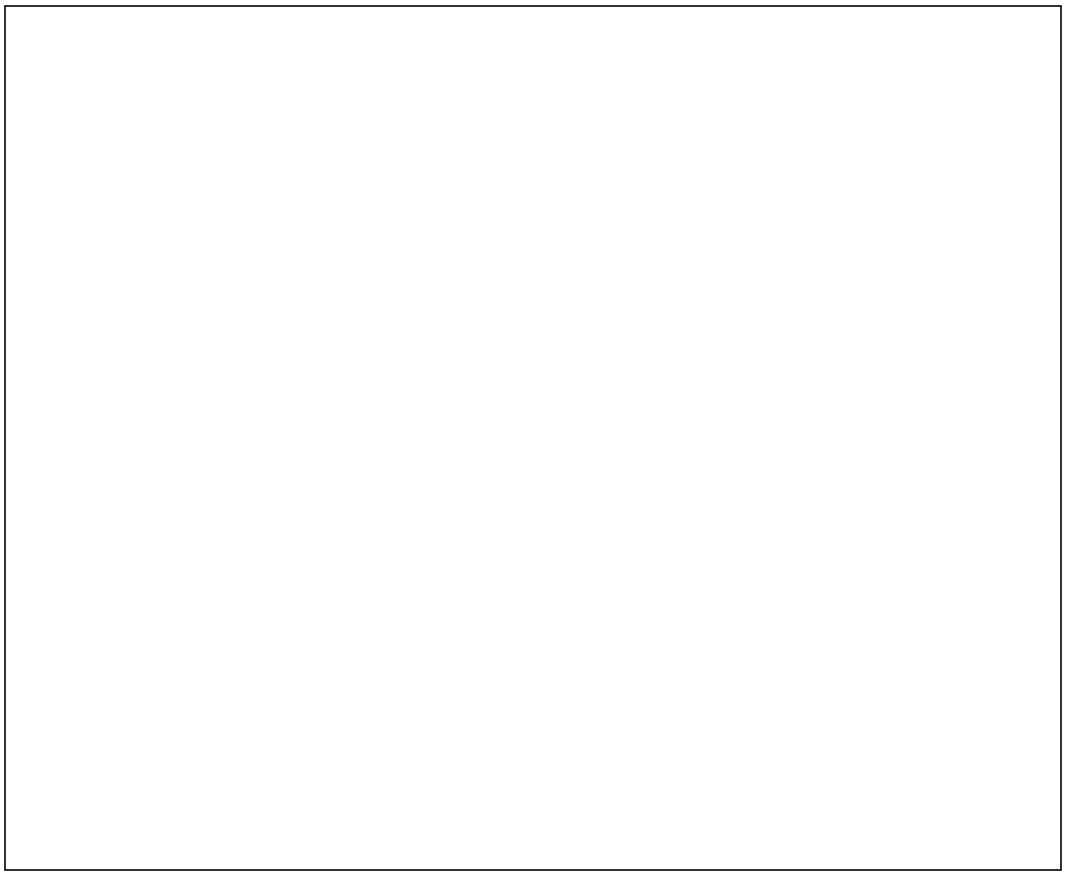
Reduce the K-map by grouping the 1's and produce optimized equations:

S =

CO =

<Part G>

Using the equation draw the Logics for S and Co:



<Part D>

Create Truth Table

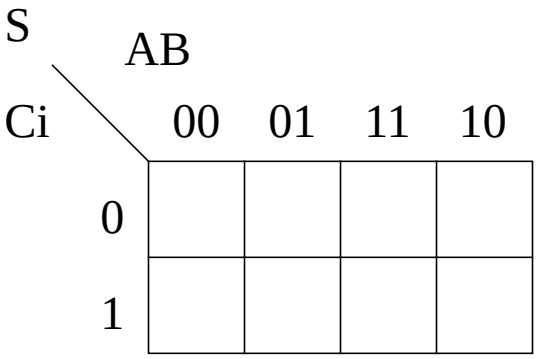
What do you think the figure 1 logic is for?

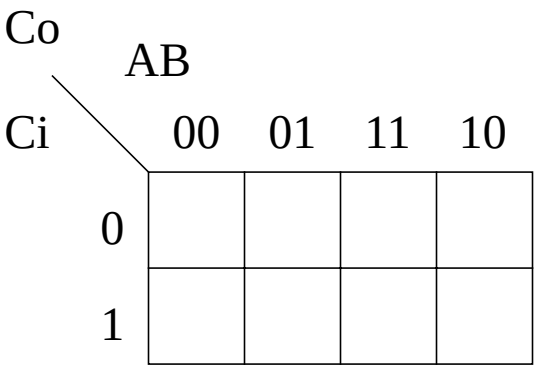
Table 1: Truth Table

A	B	Ci	S	Co

<Part E>

Fill in the K-map below:





<Part B>

Change the logic in Figure 1 in terms of NOR gates:
For Example: Buffer can be made with NOR gate with its input tied together.

<Part C>

Change logic design into equations in reduced form:
For Example: (A+B) C = AC + BC

S =

CO =

Logic Design Worksheet

University of California at Berkeley
Department of Electrical Engineering and Computer Science
GRE Preparation Session

Group Tutor: Young H. Cho Handout 2

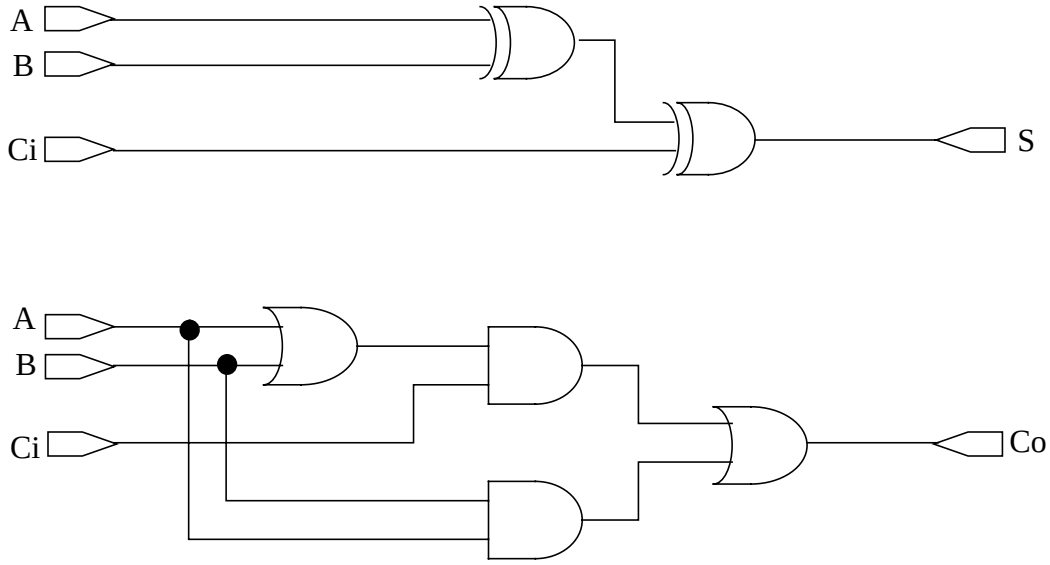


Figure 1: Questions A - E

Logic Design

<Part A>

Change the logic in Figure 1 in terms of NAND gates:
For Example: Inverter can be made with NAND gate with its input tied together.