Optimized Automatic Target Recognition Algorithm on Myrinet/FPGA Nodes

Young H.Cho
Embedded Signal Processing Laboratory
The University of Texas at Austin
Austin, TX 78712 U.S.A.
young@ece.utexas.edu

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Two-level Multicomputer

- Two levels of processor
  - First-level processor for communication
  - Second-level processor for computation
- Open message passing network
  - Low software overhead in message handling
  - Rapid insertion of commodity technology (DSP, general purpose processor, custom logic chip, FPGA, and etc.)

Sandia National Laboratories' Automatic Target Algorithm

- Locate and identify objects
  - Determine high probability detection
  - False alarm rate
- Hierarchical algorithm
  - Focus of Attention subsystem
  - Second-Level-Detection (FPGA nodes)

Second-Level Detection

- Match templates to given image as quickly as possible

$$SM_{x,y} = \sum_{u=0}^{31} \sum_{v=31}^{31} B_{uv} M_{x+u,y+v}$$

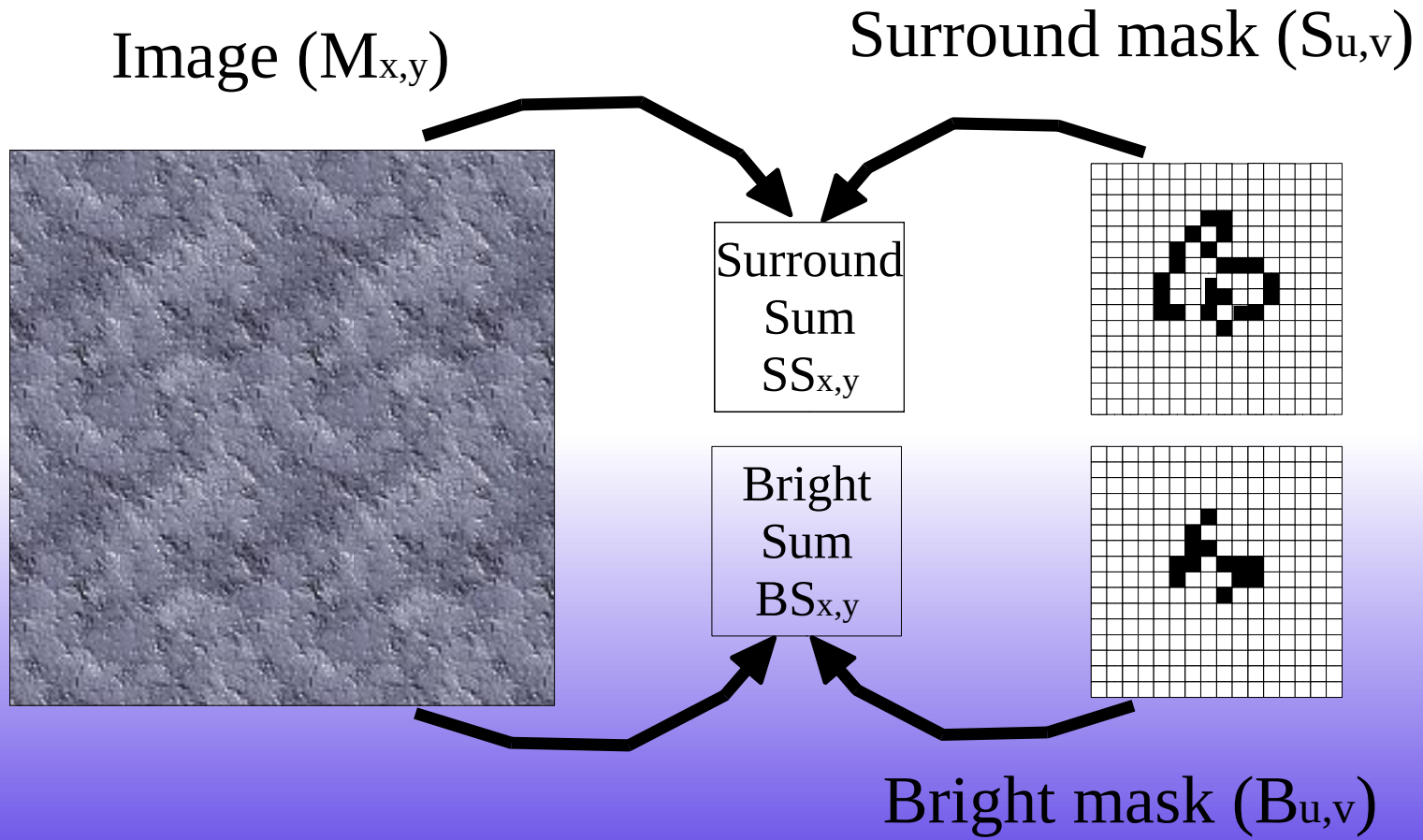
$$TH_{x,y} = \frac{SM_{x,y}}{BC} - Bias$$

$$BS_{x,y} = \sum_{u=0}^{31} \sum_{v=0}^{31} B_{u,v} \left[M_{x+u,y+v} \geq TH_{x,y} \right]$$

$$SS_{x,y} = \sum_{u=0}^{31} \sum_{v=0}^{31} S_{u,v} \left[M_{x+u,y+v} < TH_{x,y} \right]$$

$$Q_{x,y} = \frac{1}{2} \left(\frac{BS_{x,y}}{BC} + \frac{SS_{x,y}}{SC} \right)$$

Image correlation



Understanding the algorithm

U_0: $SM_{00}=B_{00}M_{00}+B_{01}M_{01}+B_{02}M_{02}+B_{10}M_{10}+B_{11}M_{11}+B_{12}M_{12}+B_{20}M_{20}+B_{21}M_{21}+B_{22}M_{22}$

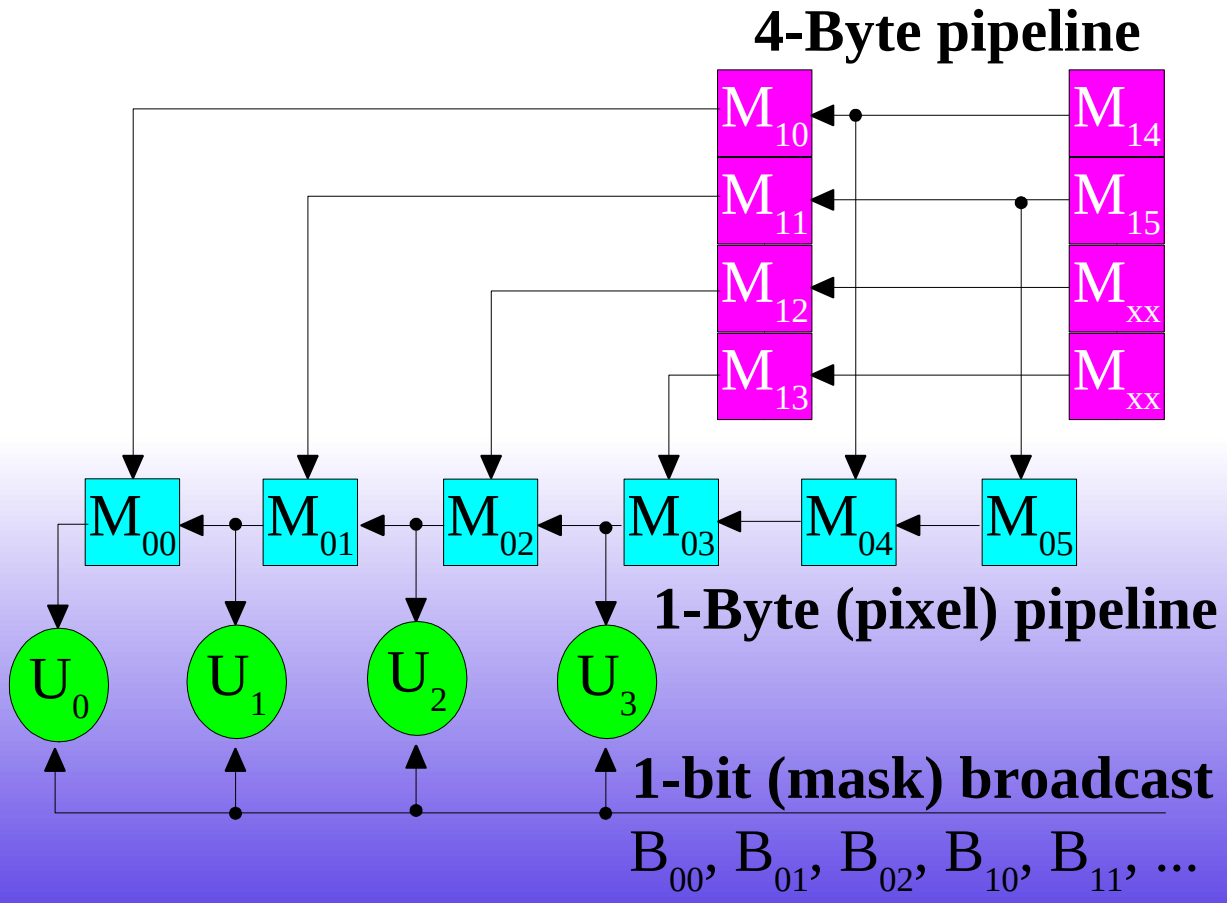
U_1: $SM_{01}=B_{00}M_{01}+B_{01}M_{02}+B_{02}M_{03}+B_{10}M_{11}+B_{11}M_{12}+B_{12}M_{13}+B_{20}M_{21}+B_{21}M_{22}+B_{22}M_{23}$

U_2: $SM_{02}=B_{00}M_{02}+B_{01}M_{03}+B_{02}M_{04}+B_{10}M_{12}+B_{11}M_{13}+B_{12}M_{14}+B_{20}M_{22}+B_{21}M_{23}+B_{22}M_{24}$

U_3: $SM_{03}=B_{00}M_{03}+B_{01}M_{04}+B_{02}M_{05}+B_{10}M_{13}+B_{11}M_{14}+B_{12}M_{15}+B_{20}M_{23}+B_{21}M_{24}+B_{22}M_{25}$

- B_{uv} in n^{th} term of all the results
- M in n^{th} term of SM_{xy} is in $(n+1)^{th}$ term of SM_{xy-1}

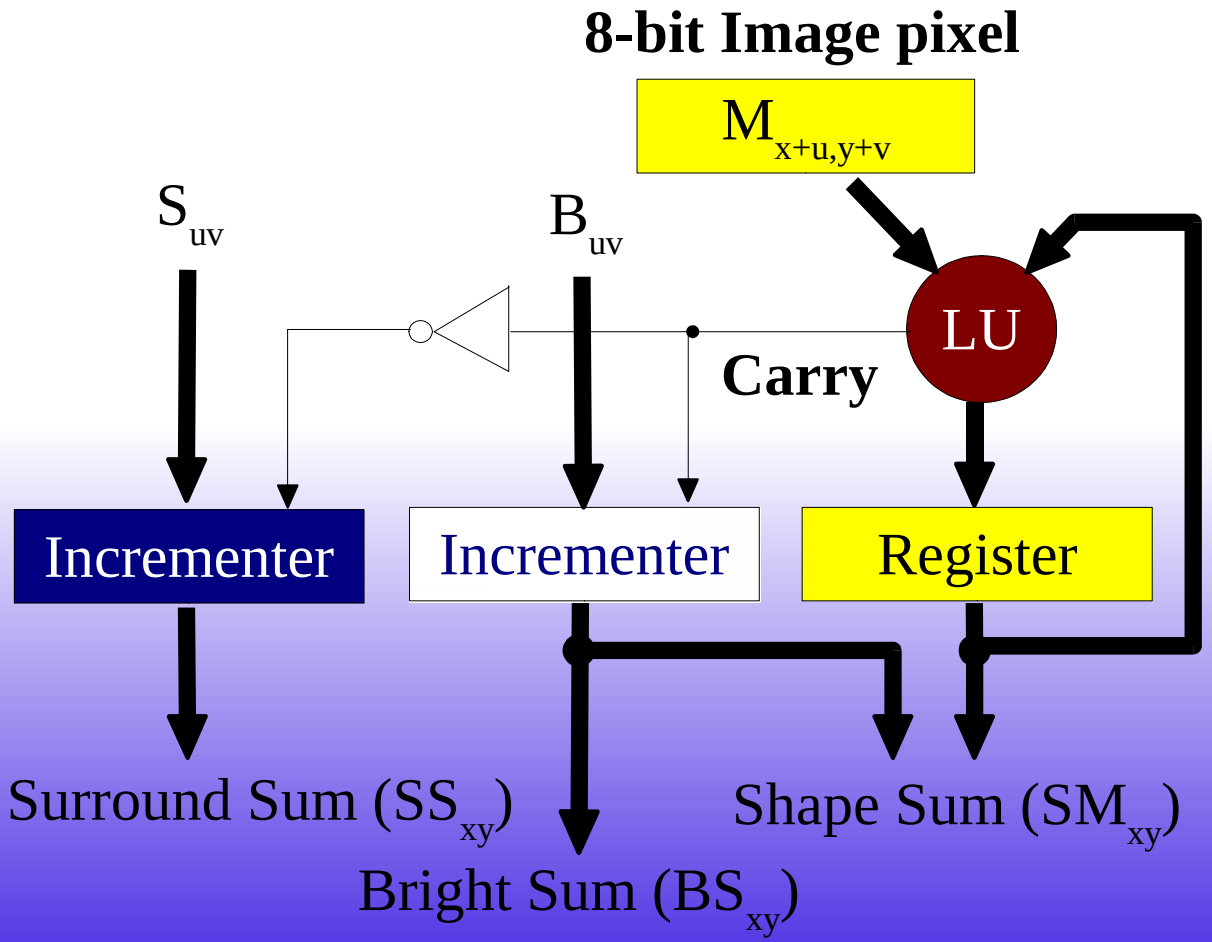
Parallel Execution



Computational tasks

- The result (U) is in function of image pixel (M) and mask bit (B or S)
- Adding 8-bit number to 16-bit number is equivalent to adding two lower 8-bit numbers and incrementing the higher 8-bit number of the 16-bit with carry out
- BS equivalent to adding 8-bit image with negated threshold(-TH) then incrementing using the carry out

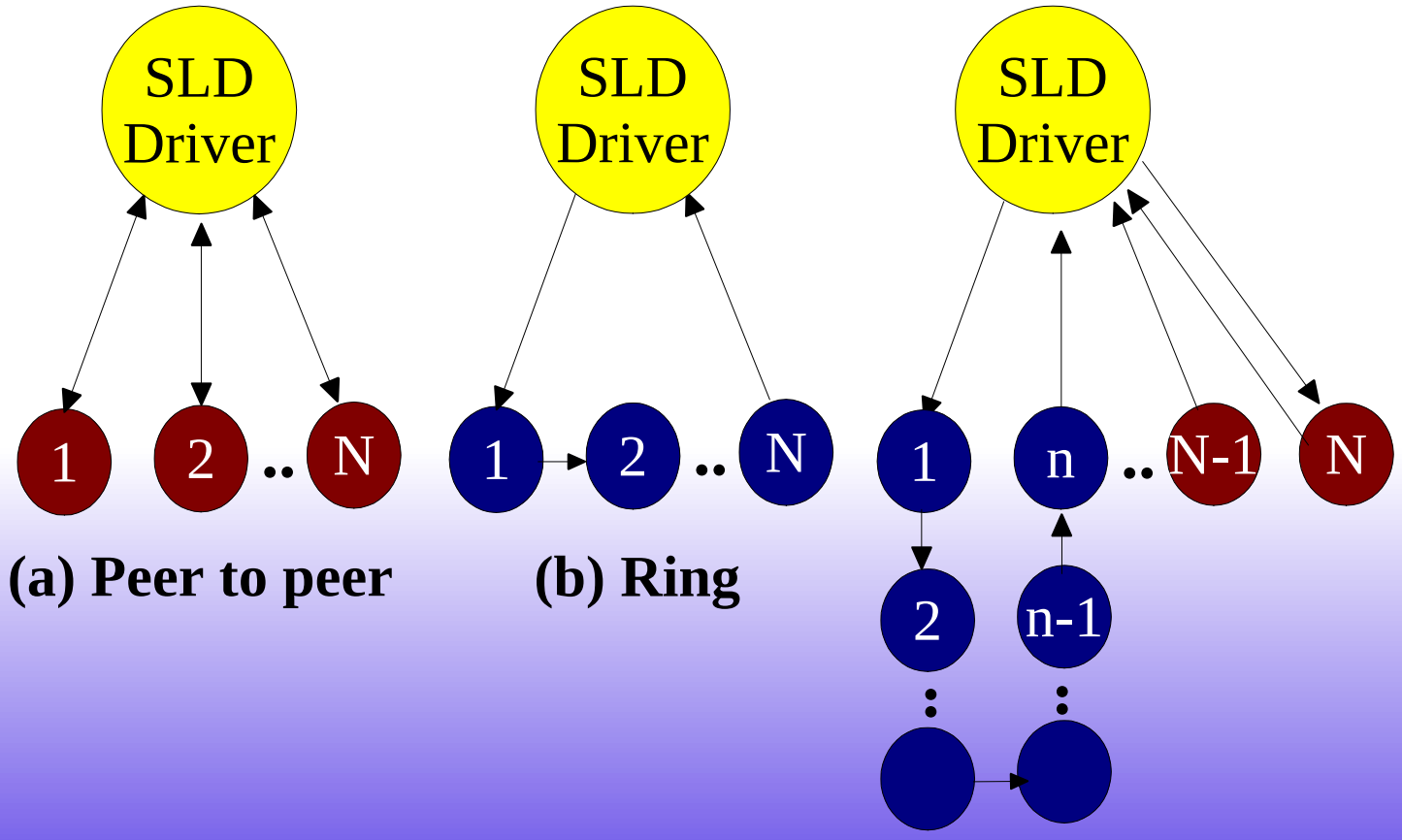
Computation Logic Unit



Scalable system

- Independent computation nodes
  - All the template data in the memory
  - Fault tolerant
  - Efficient computation
- Ring topology
  - Distributed template data
  - Passing only the best two matches
- Combining both topologies

ATR System Topology



Performance

- Without optimization
  - Over 900 templates per second per node
  - If we consider *1-bit conditional accumulate, subtract, divide, multiply, and byte compare* as one operation: 2.8 billion 8-bit operations/second (GOPS).
- With optimization
  - Skip zero mask rows: 4.0 GOPS (measured)
  - Other optimization simulation: 7.75 GOPS

Conclusion

- High-bandwidth scalable system
  - Readily interconnected via Myrinet
  - Object oriented hardware design

    (Two-level multicomputer architecture)
- Reconfigurable system
  - Modifications for the computations are isolated to the FPGA program
  - Same fast hardware with different algorithms